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| 10/775,448 | 02/10/2004 | James R. Goodman | 1512.019 | 9410 |

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| EXAMINER | |
|---|---|
| VO, THANH DUC | |
| **ART UNIT** | **PAPER NUMBER** |
| 2189 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@boylefred.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/775,448 | GOODMAN ET AL. | |
| | Examiner | Art Unit | |
| | Thanh D. Vo | 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is responsive to the Amendment filed on April 6, 2007.

### *Claim Objections*

2. Claims 1-20 are objected to because of the following informalities:

As per claim 1, the limitation ii should be written as – "in the event of a conflict with another processor unit executing the critical section and needing to write data within the critical section, establishing a priority between the processor units and another processor unit to resolve the conflict without acquisition of the lock."

As indicated by Applicant in the page 8 of the remark, "the processor units" refer to two processor units trying to execute the critical section, wherein the processor units are "another processor unit" and "the processor unit". The amendment suggest above will remove the ambiguity caused by the component "processor units" since "the processor units" per se would be lacking the antecedent basis.

As per claim 2, the phrase "and where the conflicts resolution circuit establishes a priority between the processor units by:" in lines 3-4 should be written as – "and where the conflicts resolution circuit establishes a priority between the processor units and another processor unit by:"

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 6, the paragraph [0021] in the specification rather discloses the globally unique clock **includes** a time variant field and a static processor-unit-dependent field instead of the clock with a globally unique clock value **provides** a time variant field and a static processor-unit-dependent field.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 10, 11, 16, 17-20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivas et al. in view of Applicant Admitted Prior Art (herein after AAPA).

As per claims 1 and 23, Srinivas et al. discloses a processor unit for a shared-memory computer comprising:

a processor unit (Fig. 3, item 300);

a local memory system executing a protocol to share data with at least one other processor unit (col. 6, lines 19-23);

a conflicts resolution circuit executing a hardware program to:

(i) detect a critical section in an executing program and executing the critical section without acquisition of a lock (col. 2, lines 66 – col. 3, lines 1, wherein the data elements are in the critical section since the critical section is where shared data are stored);

(ii) in the event of a conflict with another processor unit executing the critical section and needing to write to data within the critical section (col. 7, lines 48-52), establishing a priority between the processor units to resolve the conflict without acquisition of the lock. See col. 4, lines 15-27, wherein the protocol of LIFO or FIFO inherently sets the priority of the requests from the processor units.

Although Srinivas et al. does not particularly teach a speculative execution. However, AAPA teaches a speculative execution on paragraph [0008] of US application number 10/037,041. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Srinivas et al. to execute the speculative execution. The motivation of doing so is save the wasted time in running the unnecessary lock and unlock routines that may lead to inefficient

system of operation (Srinivas et al., col. 7, lines 44-46) when the system is executing the speculative executions.

As per claim 10, Srinivas et al. discloses wherein the confliction resolution circuit further executes the hardware program to:

(iv) read the buffered deferred requests at a time after the deferring to release data to the other processor unit. See col. 7, lines 47-56, wherein the atomic operation of CAS (compare-and-swap) removes the deferred requests out of the queue to be executed once the resource is available.

As per claim 11, although Srinivas et al. does not explicitly disclose a critical section detection circuit detecting the start and end of execution by the processor of a critical section of a program subject to a lock and wherein the later time is the completion of a critical section; however, detecting the start and end of execution and the ending time of an instruction are well known features in the computer art to determine when to begin the execution and to end the execution. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's to have a circuit to detect the start and end of the execution in order to avoid the wasted clock cycles that were not required in order to execute the instruction from the processor.

As per claim 16, Srinivas et al. discloses a processor unit further including:

a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock and (ii) execute the critical section without acquiring the lock (col. 2, lines 66 – col. 3, lines 1, wherein the data elements are in the critical section since the critical section is where shared data are stored);

(iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned by the processor unit (col. 7, lines 30-35); and

(iv) when no conflict for data of the critical section is detected, commit the execution of the critical section is an inherent feature of Srinivas et al. because the design of Srinivas et al. to allow the processor to access the shared memory if there is no contention between the processors.

Although Srinivas et al. does not particularly teach a speculative execution. However, AAPA teaches a speculative execution on paragraph [0008] of US application number 10/037,041. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Srinivas et al. to execute the speculative execution. The motivation of doing so is save the wasted time in running the unnecessary lock and unlock routines that may lead to inefficient system of operation (Srinivas et al., col. 7, lines 44-46) when the system is executing the speculative executions.

As per claim 17, Srinivas et al. discloses a conflict resolution circuit allows continued speculation execution of the critical section when the conflict is resolved by deferring the release of the data. See col. 3, lines 1-14, wherein the conflict is resolved and the speculation execution can be continued when the CAS is done swapping or deferring the conflicted request so that the incoming request which has a higher priority can be executed.

As per claim 18, Srinivas et al. does not explicitly disclose a method of ceasing of the speculative execution of the critical section when the conflict is resolved by releasing the data. However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that a speculative execution is considered to be completed once the conflict circuit has resolved the contention by releasing the data required by that speculative execution. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that the speculative execution should be ended or ceased once it is completed in order to allow the next execution to be completed.

As per claim 19, Srinivas et al. discloses wherein the confliction resolution circuit further executes the hardware program to:

(iv) read the buffered deferred requests at a time later to release data to the second processor unit. See col. 7, lines 47-56, wherein the atomic operation of CAS

(compare-and-swap) removes the deferred requests out of the queue to be executed once the resource is available.

Although Srinivas et al. does not explicitly disclose a method of ceasing the speculation execution of the critical section when buffer memory is exhausted; however, it is well known in the computer art that once the memory buffer is full or exhausted then it should be ceased until the buffer memory is available again. The motivation of doing so is to allow the previous instruction to be finished since the result of previous instruction could be needed or used by the incoming instructions that are after it.

As per claim 20, Srinivas et al. teaches a processor unit including a buffer memory. See col. 3, lines 3-7.

However, Srinivas does not specifically disclose a buffer memory to store the results of speculation and ceasing the speculative execution of the critical section when the buffer memory is exhausted.

However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to use a buffer memory to store the result of an execution before the result of the execution is written to physical memory. The motivation of doing so is to temporarily storing the data while waiting the data bus is busy in order to avoid the data loss.

In addition, it is well known in the computer art that once the memory buffer is full or exhausted then it should be ceased until the buffer memory is available again. The

motivation of doing so is to allow the previous instruction to be finished since the result of previous instruction could be needed or used by the incoming instructions that are after it.

5. Claims 2, 3, 5, 6-8, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivas et al. (US Patent 6,651,146) and Applicant Admitted Prior Art (herein after AAPA) in view Massalin et al. (Publication of Columbia University)

As per claim 2, a globally unique clock is an inherent feature in the system of Srinivas et al. because a system has to have a timing circuit in order to schedule and determine the speed which the instructions are executed;

Srinivas et al. further teach a processor unit further including:

a conflicts resolution circuit establishes a priority between the processor units by:

(b) releasing owned data requested by a second processor unit making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the first processor unit (col. 3, lines 1-14, wherein the access request from the processor A (300) or processor B (301) to the shared memory (303) is queuing into a FIFO queue which is a first come first serve fashion); and

(c) deferring release of owned data requested by the second processor unit making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the first processor unit. See col. 3, lines 1-14; since a FIFO is a first come first serve fashion, therefore the whichever the access request that

arrives at the later time than the previous one is queuing or deferring into the FIFO queue while waiting for the one ahead of it to be finished.

Srinivas et al. does not explicitly teach the following feature:

(a) time stamping requests for data sent by a first processor unit to other processor units with a value of the globally unique clock;

However, Massalin et al. discloses a method of scheduling using a global counter and priority table to indicate the queue level of each access request, wherein the priority table contains scheduling policy that assign to each of the request entry. See page 8, section 4.1, lines 1-3 of third paragraph, and fourth paragraph.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Srinivas et al. to include the teaching of Massalin et al. in order to arrive at the current invention. The motivation of doing so is to have a time stamping (scheduling using system generated time) method to further enhance determine the priority of the request entry not just simply by the arrival of the request but the time of the request was generated in order to orderly queuing the request into the FIFO taught by Srinivas et al.

As per claim 3, since there is no elaboration in the invention of Srinivas et al. to indicate that the conflict resolution circuit is to be used anywhere else rather than the critical section that resides in the shared memory to prevent the contention for the access to the shared memory; therefore, it is readily apparent that Srinivas et al.

discloses a processor unit wherein the conflicts resolution circuit executes hardware program step (i) **only** during execution of a critical section because

As per claim 5, although Srinivas et al. did not specifically teach a cache coherence protocol. However, AAPA discloses a cache coherence protocol on paragraph 0044, last sentence. As stated in the Specification, a cache coherence protocol is a well known in the art. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to use the Srinivas et al.'s invention in combination with the cache coherence protocol to arrive at the current invention. The motivation of doing so is to allow the cache from the processors A and B of Srinivas et al. to orderly access the shared data while avoiding the dead cycle dues to access conflicts or contentions.

As per claim 6, a time variant field and static processor-unit-dependent filed in a processor unit is an inherent feature in the processor unit of Srinivas et al. because a processor has to execute the instructions or processes in a clock cycle fashion, wherein the clock is increment according to time.

As per claim 7, Massalin et al. discloses processor unit of wherein the globally unique clock is a counter updated after executions by the processor of a critical section of a program subject to a lock. See page 8, section 4.1, last paragraph, wherein the

processor is subject to lock since the lock-based algorithm can be use to solve the contention issue otherwise.

As per claim 8, Massalin et al. discloses processor unit wherein the counter sets itself to a higher number on updating. See page 8, section 4.1, last paragraph, lines 1-4.

As per claims 21 and 22, Srinivas et al. discloses a processor unit system comprising: a plurality of processor units (col. 4, lines 7-10) having:

a processor unit;

a local memory system (col. 4, lines 7-10, shared memory) executing a protocol to share data with at least one other processor unit;

a globally unique clock is an inherent feature in the system of Srinivas et al. because a system has to have a timing circuit in order to schedule and determine the speed which the instructions are executed;

Srinivas et al. further teach a processor unit further including:

a conflicts resolution circuit establishes a priority between the processor units by:

(b) releasing owned data requested by a second processor unit making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the first processor unit (col. 3, lines 1-14, wherein the access request from the processor A (300) or processor B (301) to the shared memory (303) is queuing into a FIFO queue which is a first come first serve fashion); and

(c) deferring release of owned data requested by the second processor unit making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the first processor unit. See col. 3, lines 1-14; since a FIFO is a first come first serve fashion, therefore the whichever the access request that arrives at the later time than the previous one is queuing or deferring into the FIFO queue while waiting for the one ahead of it to be finished.

Srinivas et al. does not explicitly teach the following feature:

(a) time stamping requests for data sent by a first processor unit to other processor units with a value of the globally unique clock;

However, Massalin et al. discloses a method of scheduling using a global counter and priority table to indicate the queue level of each access request, wherein the priority table contains scheduling policy that assign to each of the request entry. See page 8, section 4.1, lines 1-3 of third paragraph, and fourth paragraph.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Srinivas et al. to include the teaching of Massalin et al. in order to arrive at the current invention. The motivation of doing so is to have a time stamping (scheduling using system generated time) method to further enhance the method of determining the priority of the request entry rather than by the arrival of the request but the time of the request was generated in order to orderly queuing the request into the FIFO taught by Srinivas et al.

***Response to Arguments***

6. Applicant's arguments filed April 6, 2007 have been fully considered but they are not persuasive.

As for claim 1, Applicant argues that Srinivas fails to teach:

a) a conflict resolution circuit

b) detects a critical section

c) establishing priority between the processor units to resolve the conflict"

With respect to (a), a conflict resolution circuit is an apparent feature in Srinivas' invention because there has to have the resolution circuit in order to resolve the contention (see Abstract of Srinivas) in the invention of Srinivas.

With respect to (b), in order for the multiprocessor system to access the data elements there has to have a method to detect the shared data elements amongst the plurality of processors, wherein the data elements are the critical sections.

With respect to (c), Srinivas has to have a method to prioritize or to sort the access request of the processor units to the shared memory region.

As being mentioned by Applicant that the use of atomic instruction in Srinivas eliminates the conflict because the instruction is complete before any other instructions can interrupt it. Examiner respectfully disagree, the use of the atomic CAS (compare-and-swap) instruction of Srinivas is introduced to prevent the contention/confliction amongst the instructions. Therefore, in event that two processors A and B are to use the same data element, a priority is set in order to avoid the contention between the two processors.

As per claims 21-23, as being explained in claim 1 above, a conflict resolution circuit is an apparent feature in Srinivas' invention because there has to have the resolution circuit in order to resolve the contention (see Abstract of Srinivas) in the invention of Srinivas.

As per claims 21-22, Applicant argues that Massalin does not discloses the method of timestamping, however, the method of timestamping is equivalent to the method of scheduling using a global counter and priority table to indicate the queue level of each access request as disclosed by Massalin. Therefore, each request entry is being assigned with a global counter value and a priority value from the table to indicate the queue level of the request entry.

As per claim 23, as being explained in claim 1, in order for the multiprocessor system to access the data elements there has to have a method to detect the shared data elements amongst the plurality of processors, wherein the data elements are the critical sections.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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